Design and Optimization of Geometry Acceleration for Portable 3D Graphics

Ju-ho Sohn

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Semiconductor System Laboratory

Department of Electrical Engineering and Computer Science

Korea Advanced Institute of Science and Technology

Outline

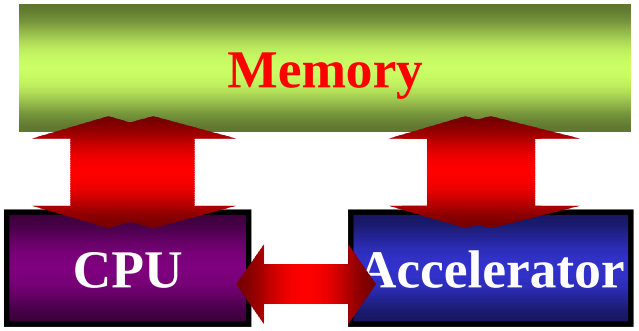
- **Introduction**
- **Design and Implementation of Bandwidth Equalizer**
- **Mobile Graphics Library**
- **Proposed 3D Geometry Coprocessor – SATINE**
- **Conclusion and Further Works**

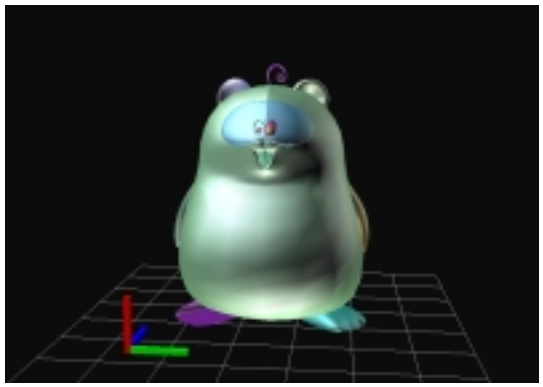
Outline

- **Introduction**
  - **Portable 3D Graphics**
  - **RAMP-IV Multimedia Processor**
  - **Problem Definitions**
  - **Performance Requirements of Mobile System**
- **Design and Implementation of Bandwidth Equalizer**
- **Mobile Graphics Library**
- **Proposed 3D Geometry Coprocessor – SATINE**
- **Conclusion and Further Works**

Introduction

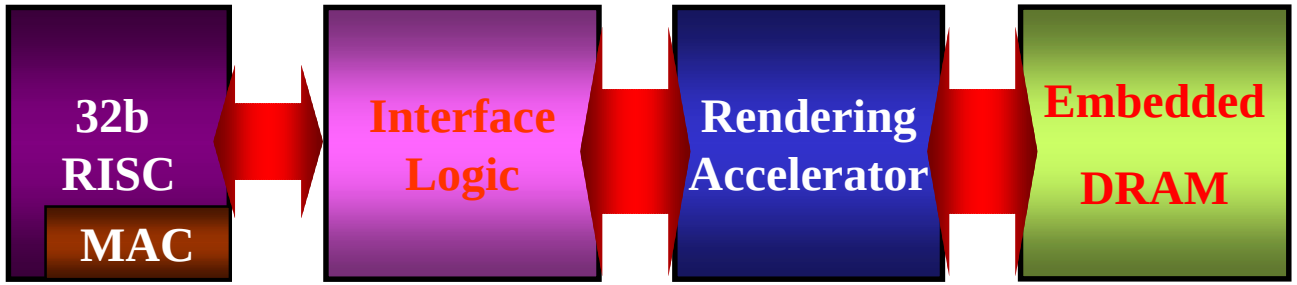
- **Portable 3D Graphics**
  - **Most attractive application**
    - **3D ad., 3D avatar and 3D game ..**
  - **Most challenging part**
    - **High computing complexity**
    - **Hugh Memory Bandwidth**
  - **Mobile System**
    - **Small screen size ⟶ Low performance requirements**

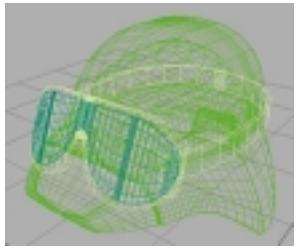




Introduction

- **RAMP-IV Portable Multimedia Processor [*]**
  - **0.16um pure DRAM process**
  - **Provide the full 3D graphics pipeline with texture mapping**





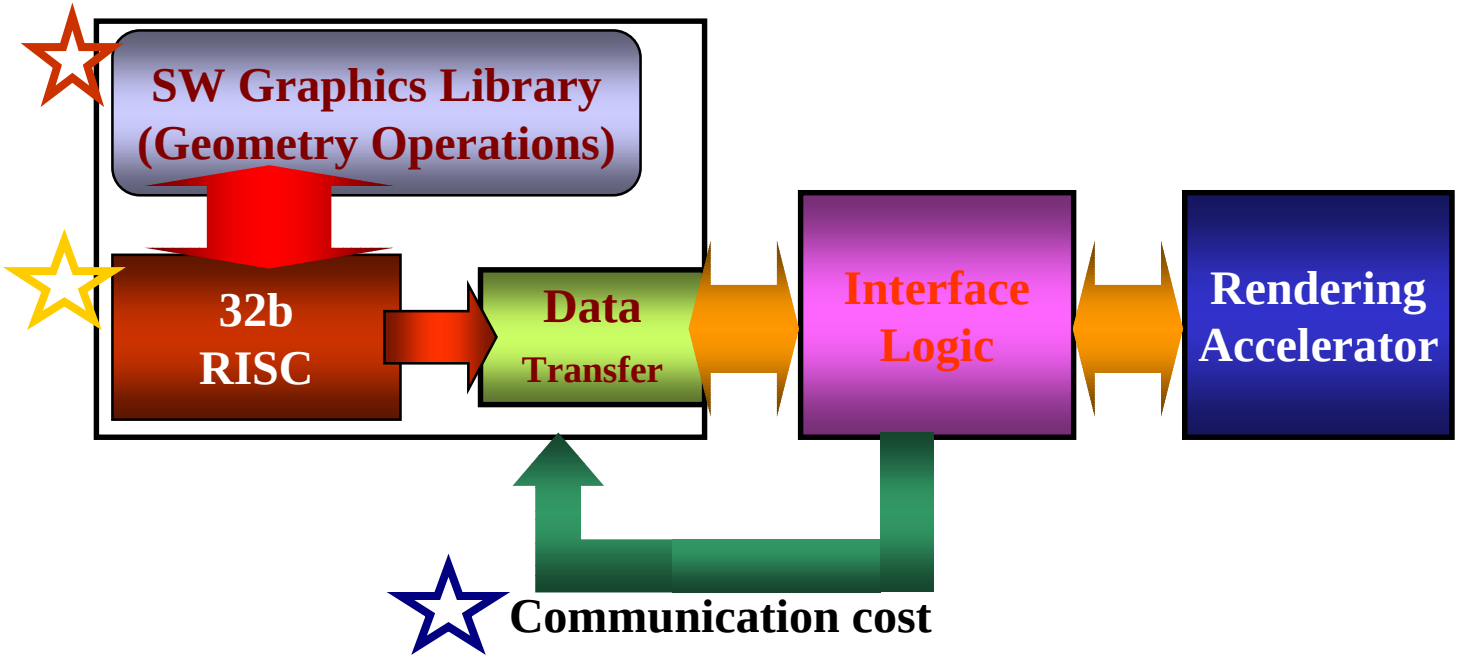
Geometry Operations

Rendering Operations

[*] R.Woo, et al, ISSCC 2003

Introduction

- **Problem Definitions**
  - **Efficient interface logic: Bandwidth Equalizer**
  - **Efficient graphics library: MobileGL**
  - **Efficient geometry accelerator: SATINE**



Introduction

- **Required Performance of Graphics System**
  - **For mobile device of 320 by 240 screen resolution**
    - **Frame rate : 15 fps for animation**
    - **Geometry stage : 144K polygon/sec**
    - **Rendering stage : 2M pixel/sec**
  - **Test Scenes**

5868 Polygons

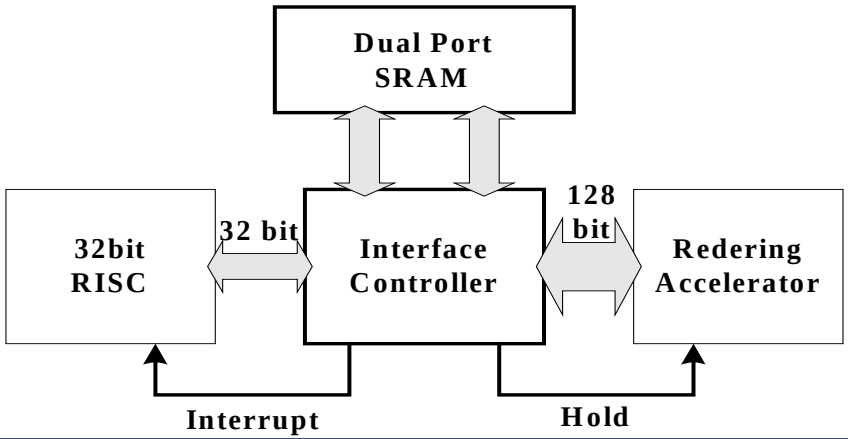
6833 Polygons

Outline

- Introduction
- **Design and Implementation of Bandwidth Equalizer**
  - **Requirements**
  - **Architecture**
  - **Chip Implementation**
  - **Performance**
- Mobile Graphics Library
- Proposed 3D Geometry Coprocessor – SATINE
- Conclusion and Further Works

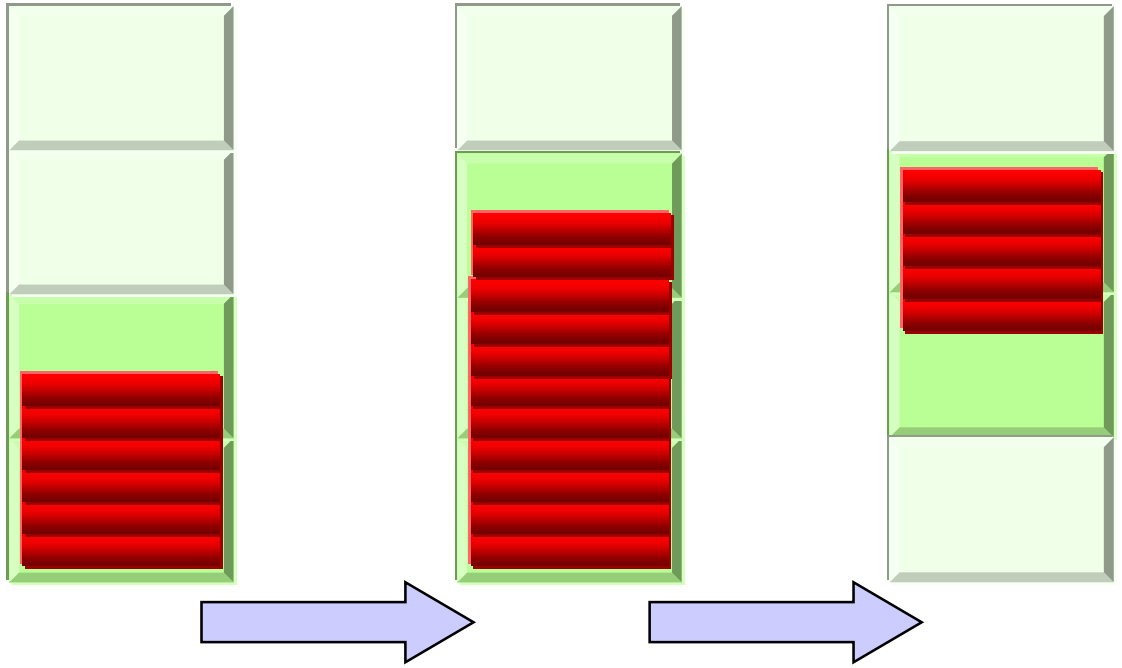
Bandwidth Equalizer

- **Requirements**
  - **Compensate the different datawidth and clock frequency**
    - **32bit input @133㎒ from RISC**
    - **128bit output @33㎒ to Rendering Accelerator**
  - **Low power consumption with reduced communication cost**
    - **Less than 5㎽**
    - **Reduce the CPU cycles for data transfer**
  - **Increase the memory utilization**



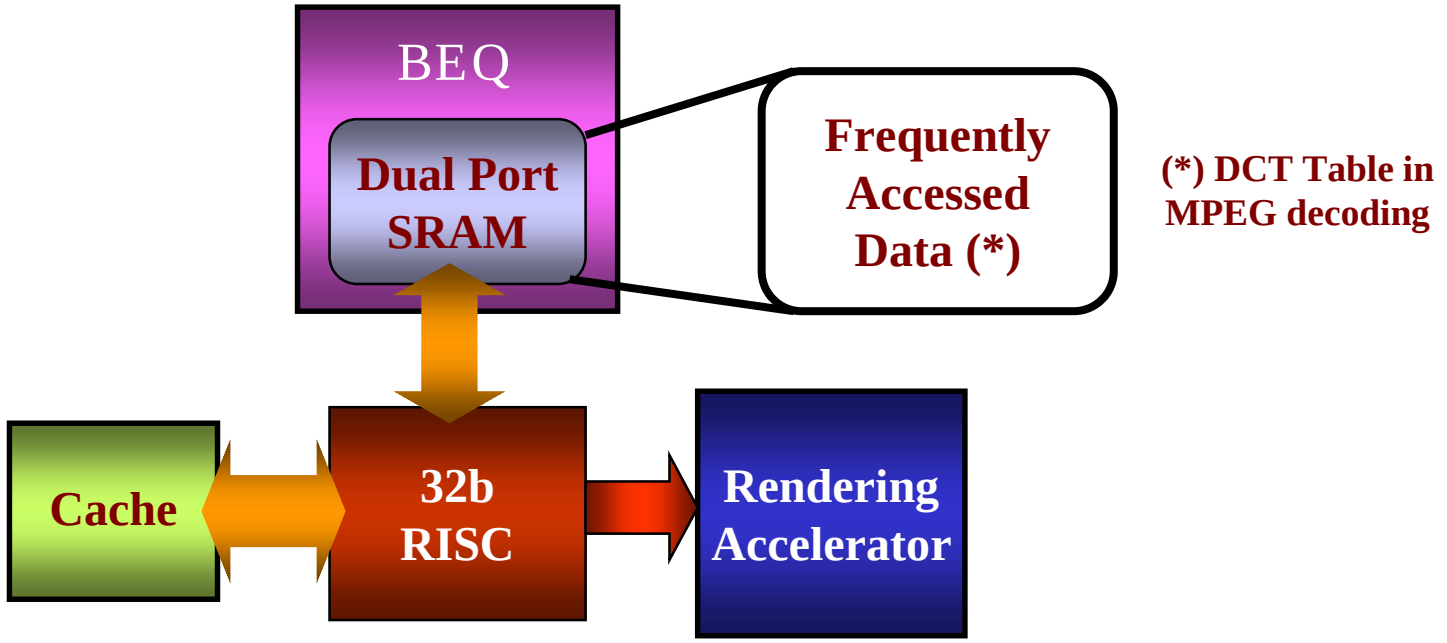
Bandwidth Equalizer

- **Architecture**
  - **Flow control**
    - **Dynamic threshold : Reduce the CPU interrupts**
    - **Adaptive bank utilization : Reduce the power consumption**



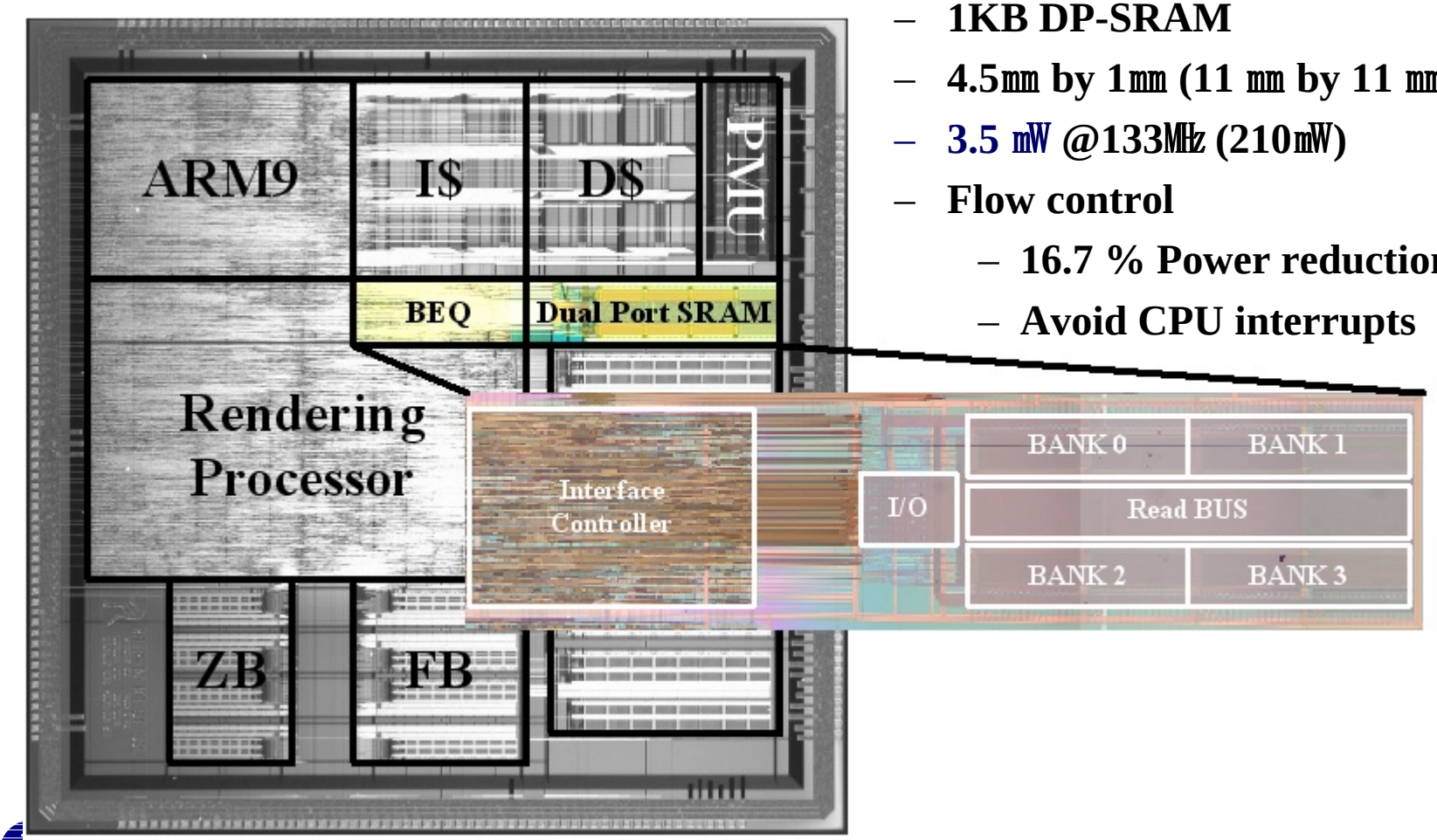
Bandwidth Equalizer

- **Architecture**
  - **Scratch Pad Memory**
    - **Increase the memory utilization**



Bandwidth Equalizer

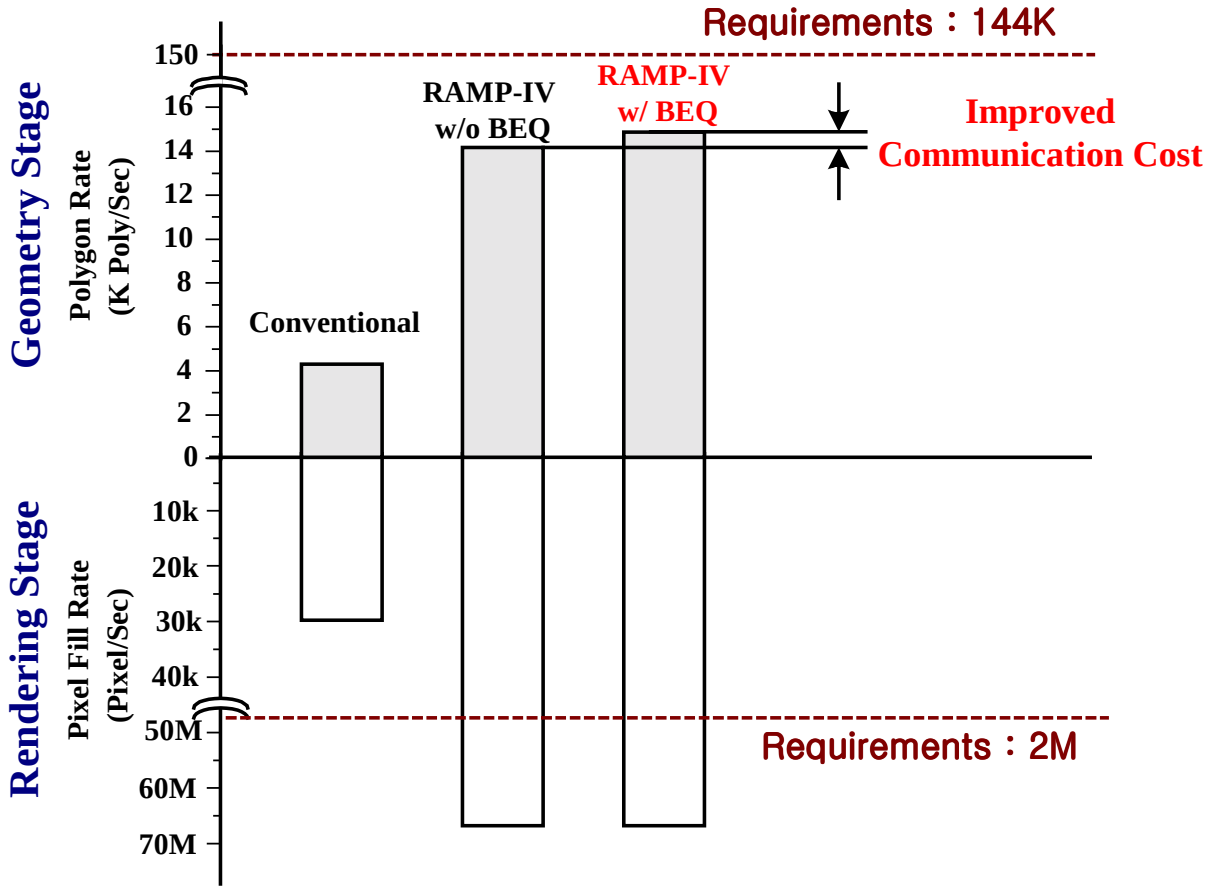
- **Chip Implementation**



- Hynix 0.16 um DRAM process
- 1KB DP-SRAM
- 4.5㎜ by 1㎜ (11 ㎜ by 11 ㎜)
- 3.5 ㎽ @133㎒ (210㎽)
- Flow control
  - 16.7 % Power reduction
  - Avoid CPU interrupts

Bandwidth Equalizer

- **Performance**



Outline

- Introduction
- Design and Implementation of Bandwidth Equalizer
- **Mobile Graphics Library (MobileGL)**
  - **Definition**
  - **Simulation Environment**
  - **Performance Result**
  - **Implementation**
- Proposed 3D Geometry Coprocessor – SATINE
- Conclusion and Further Works

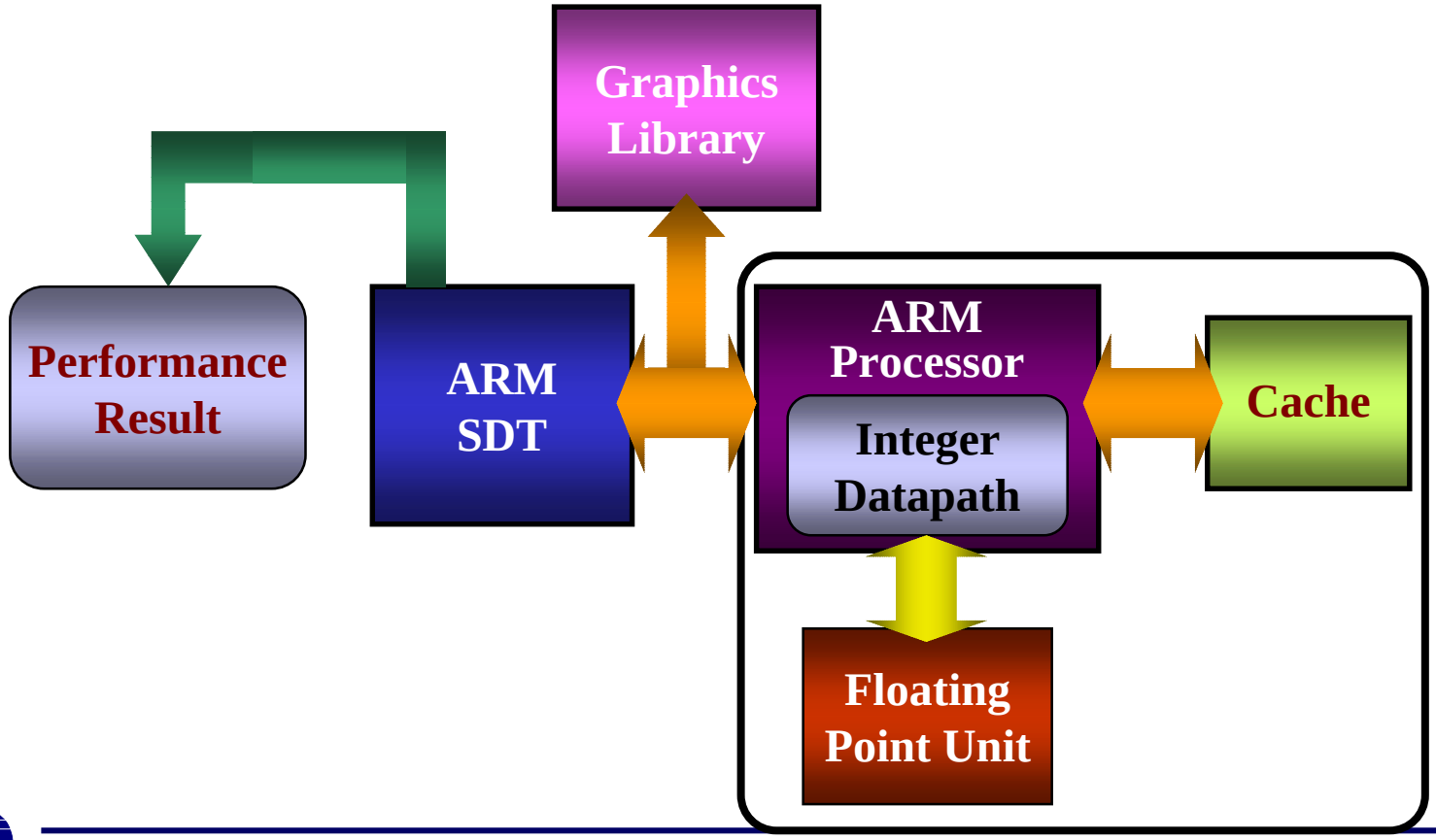
Mobile Graphics Library (MobileGL)

- **Definition**
  - **Graphics library for real time 3D graphics in mobile applications**
  - **OpenGL Compatible**
  - **Based on the optimization of graphics system for mobile applications [*]**

[*] J-H Sohn, et al, ISCAS 2002

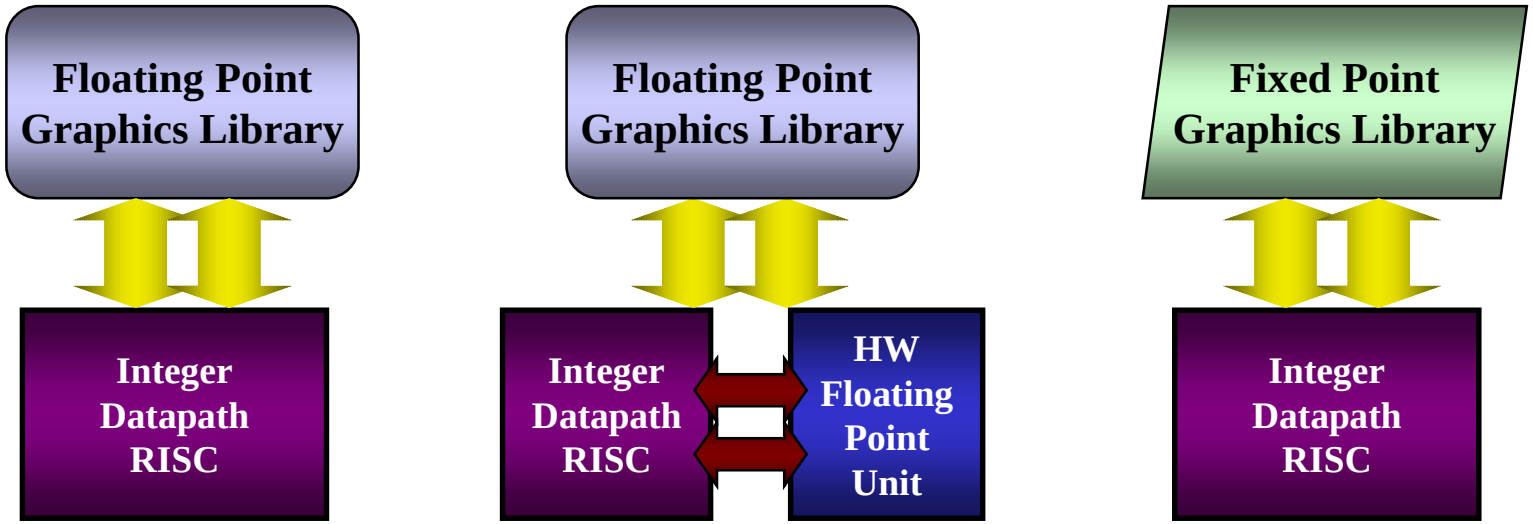
MobileGL

- **Simulation Environment**
  - **Target platform: ARM processor platform**



MobileGL

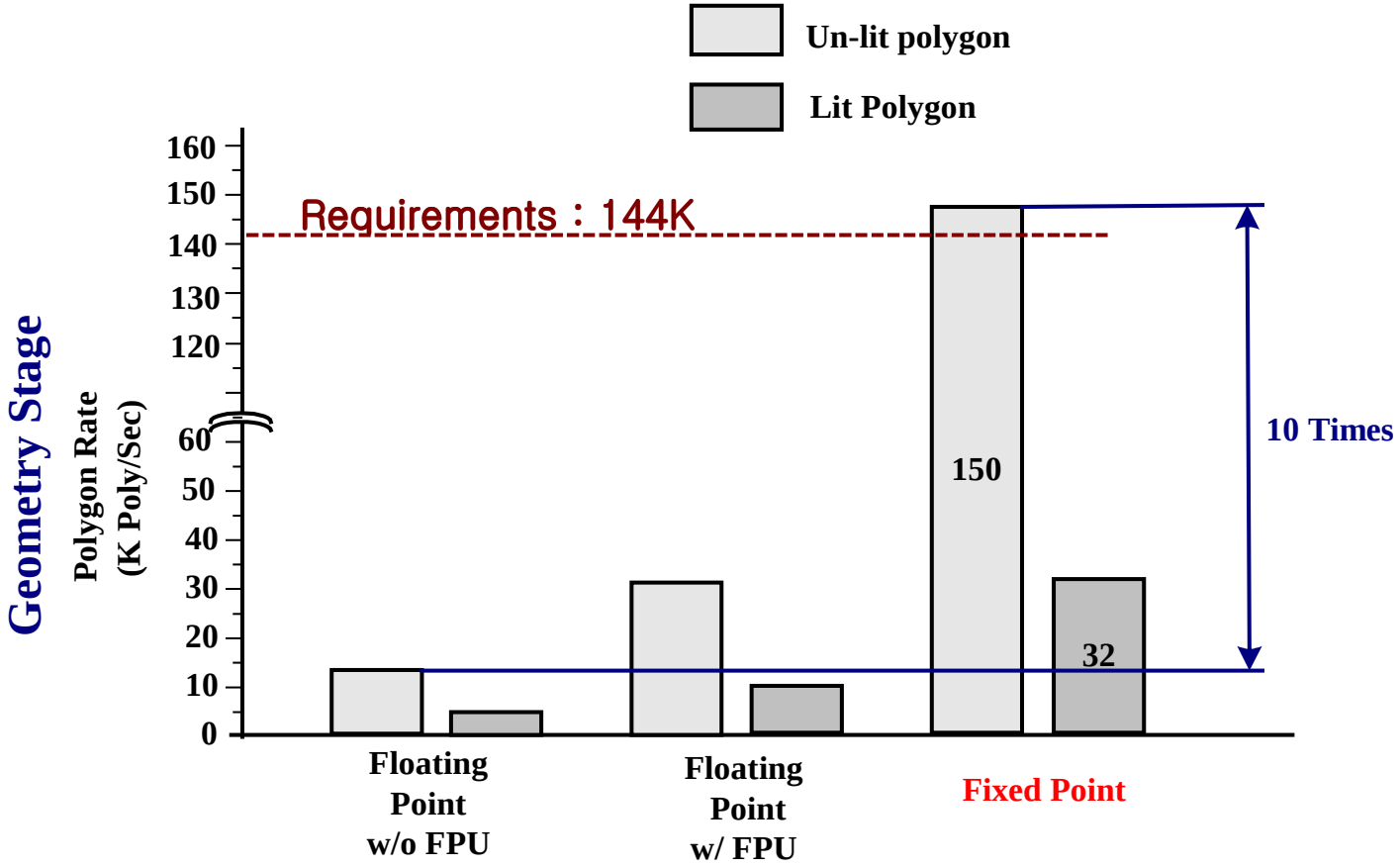
- **Target configurations**
  - **Suitable for mobile system such as PDA**
  - **Floating vs Fixed point system**



Conventional

MobileGL

- **Performance result**

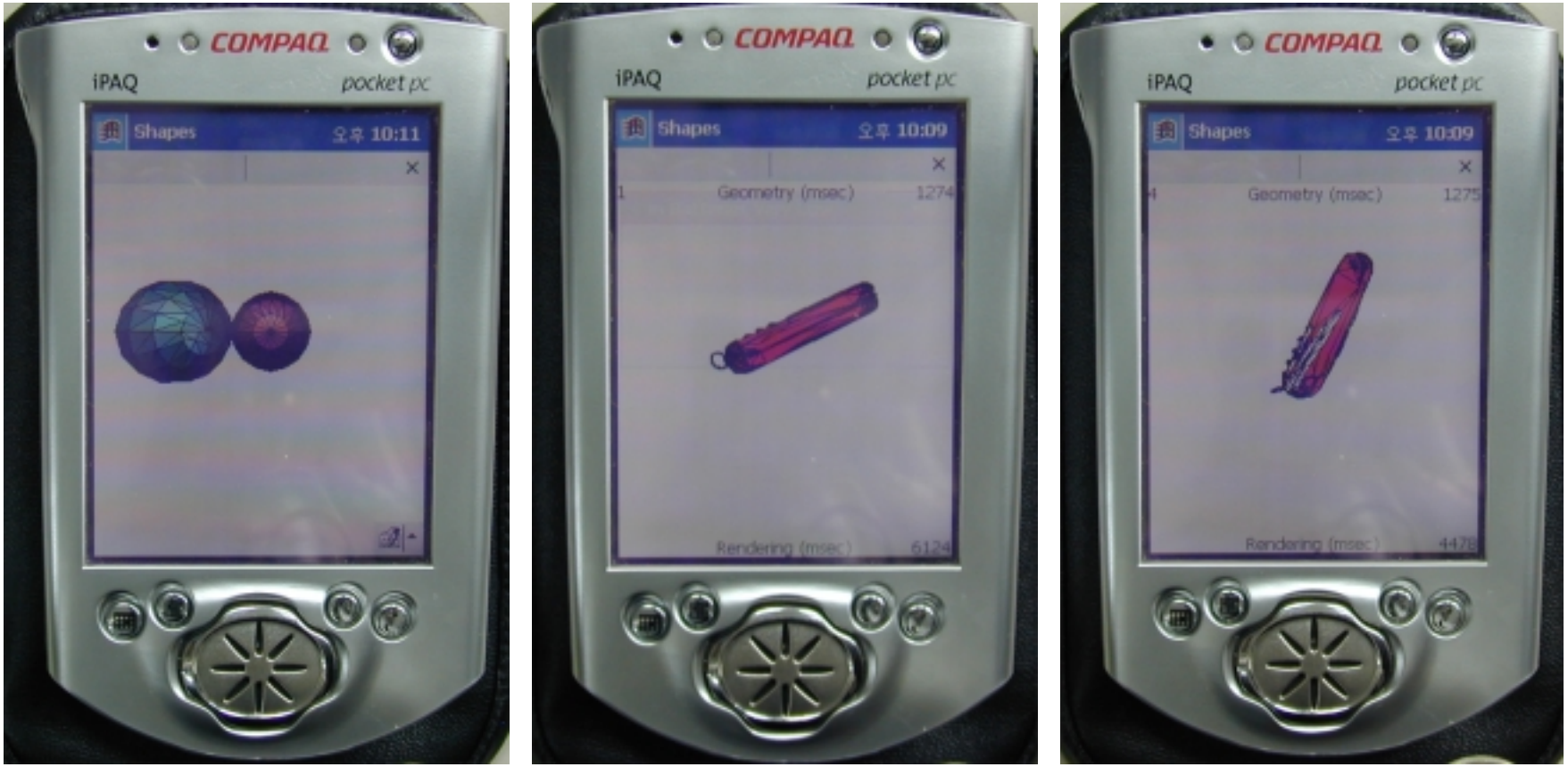


MobileGL

- **Implementation**
  - **Fixed point arithmetic**
  - **Assembly math library for SQRT/DIV**
  - **Efficient in ARM architecture**
  - **Optimized to RAMP-IV Graphics system**
    - **Geometry: ARM9 + fast MAC = 153K polygon/sec**
      - **Solve the high computing complexity**
    - **Rendering: Rendering Accelerator = 66M pixel/sec**
      - **Solve the huge memory bandwidth requirements**

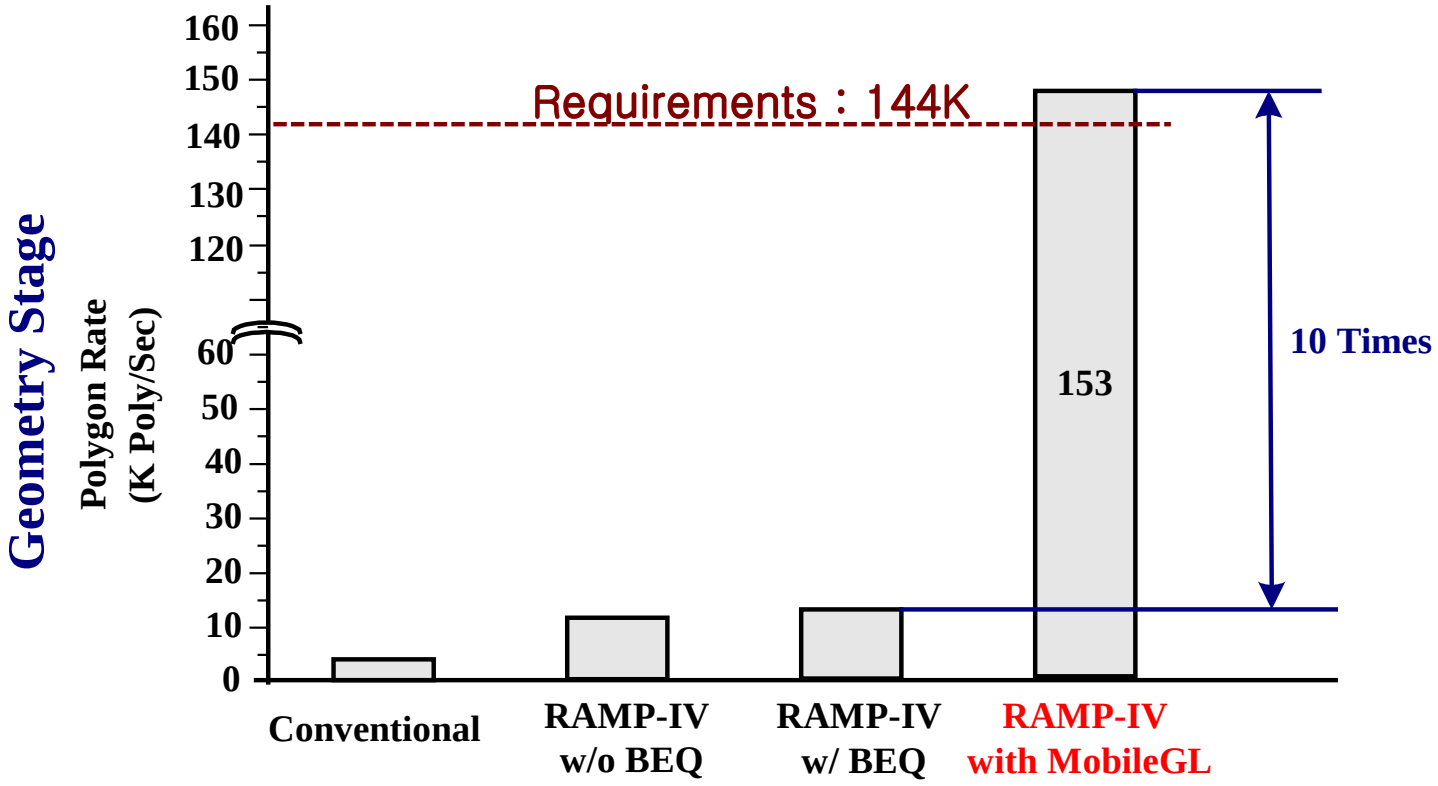
MobileGL

- **Implementation**
  - **Available on any ARM platform**



MobileGL

- **Performance Enhancement**

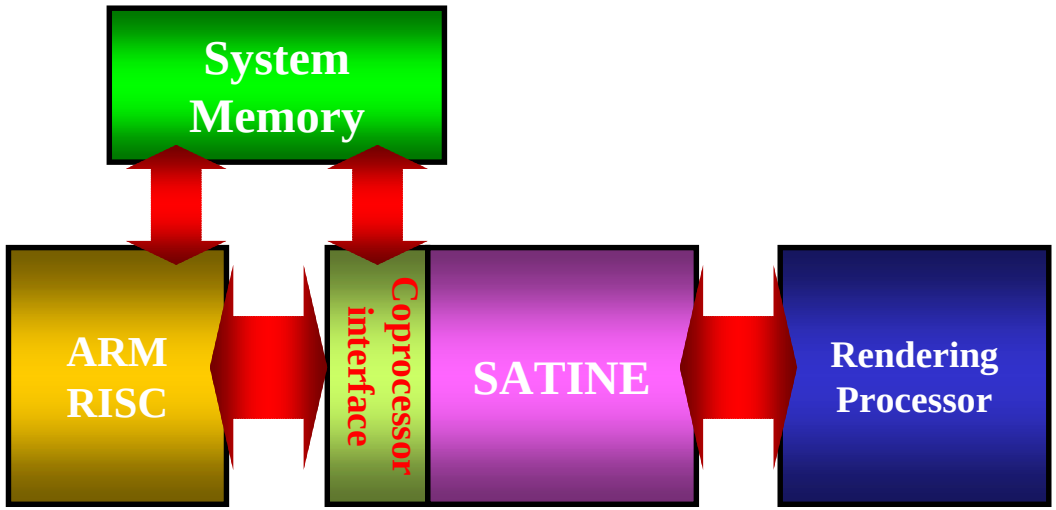


Outline

- Introduction
- Design and Implementation of Bandwidth Equalizer
- Mobile Graphics Library
- **Proposed 3D Geometry Coprocessor – SATINE**
  - **Motivation**
  - **Related Works**
  - **Architecture**
  - **Performance Estimation**
- Conclusion and Further Works

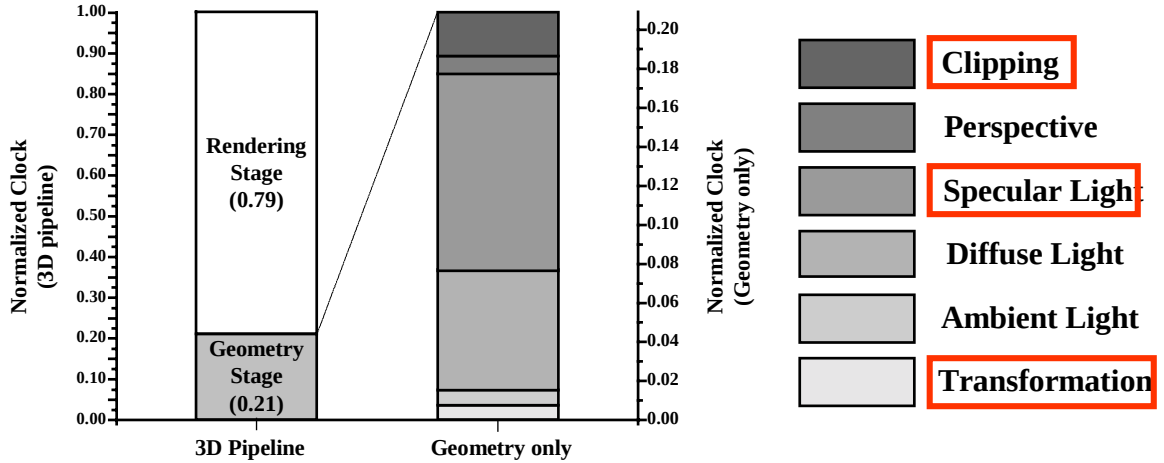
Proposed 3D Geometry Coprocessor

- **Motivation**
  - **Performance bottleneck in RAMP-IV system**
    - **Whole system is limited by Geometry Performance**
      - **Only 4~10% utilization of rendering accelerator can be obtained**
  - **For high performance with low power consumption**
    - **SATINE : Tightly coupled geometry coprocessor optimized to 3D operations**

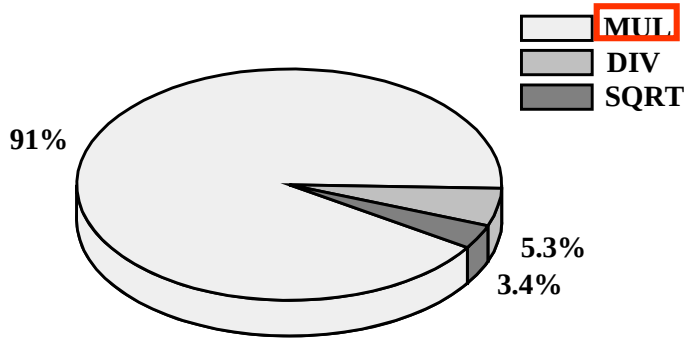


SATINE

- **Motivation (cont'd)**
  - **Cycle usages of operations in geometry stage**



  - **Operations pattern**



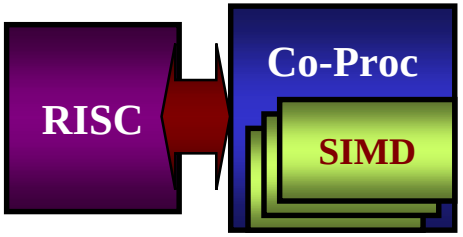
SATINE

- **Related Works**

#1 Intel GPP, 2002

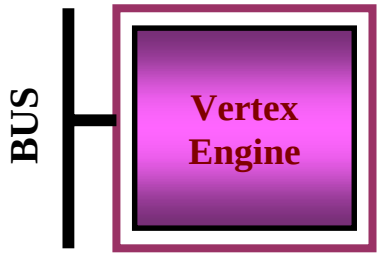
Unavoidable performance limit

#2 Intel Wireless MMX, 2202



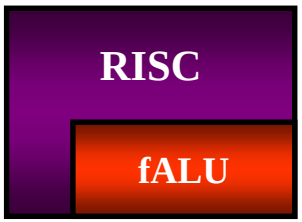
Not optimized to 3D operations

#3 PowerMBX , 2001



Complex hardware cost

#4 Mitsubishi Z-3D, 2001



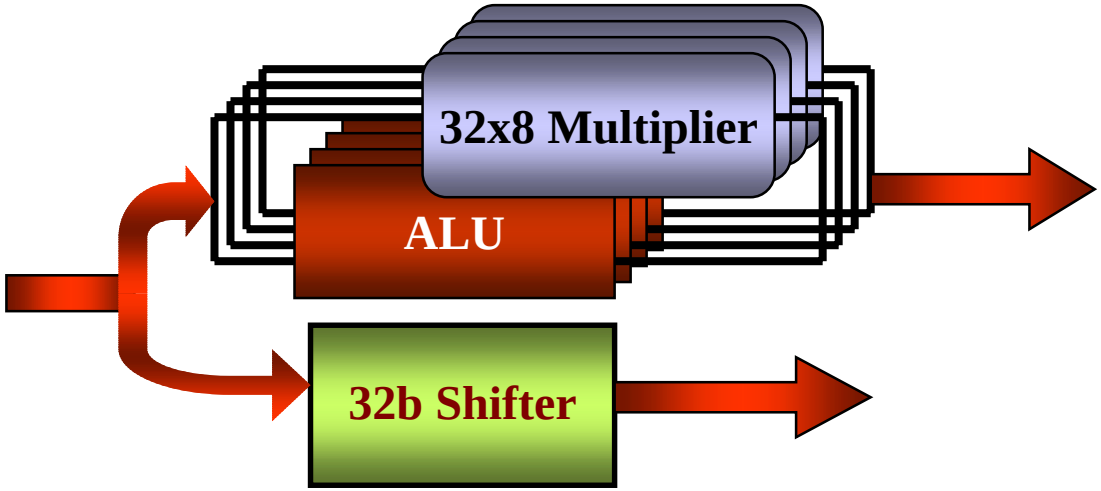
Not suitable to PDA size

#1, #2: www.intel.com

#3: www.powervr.com #4: www.melco.co.jp

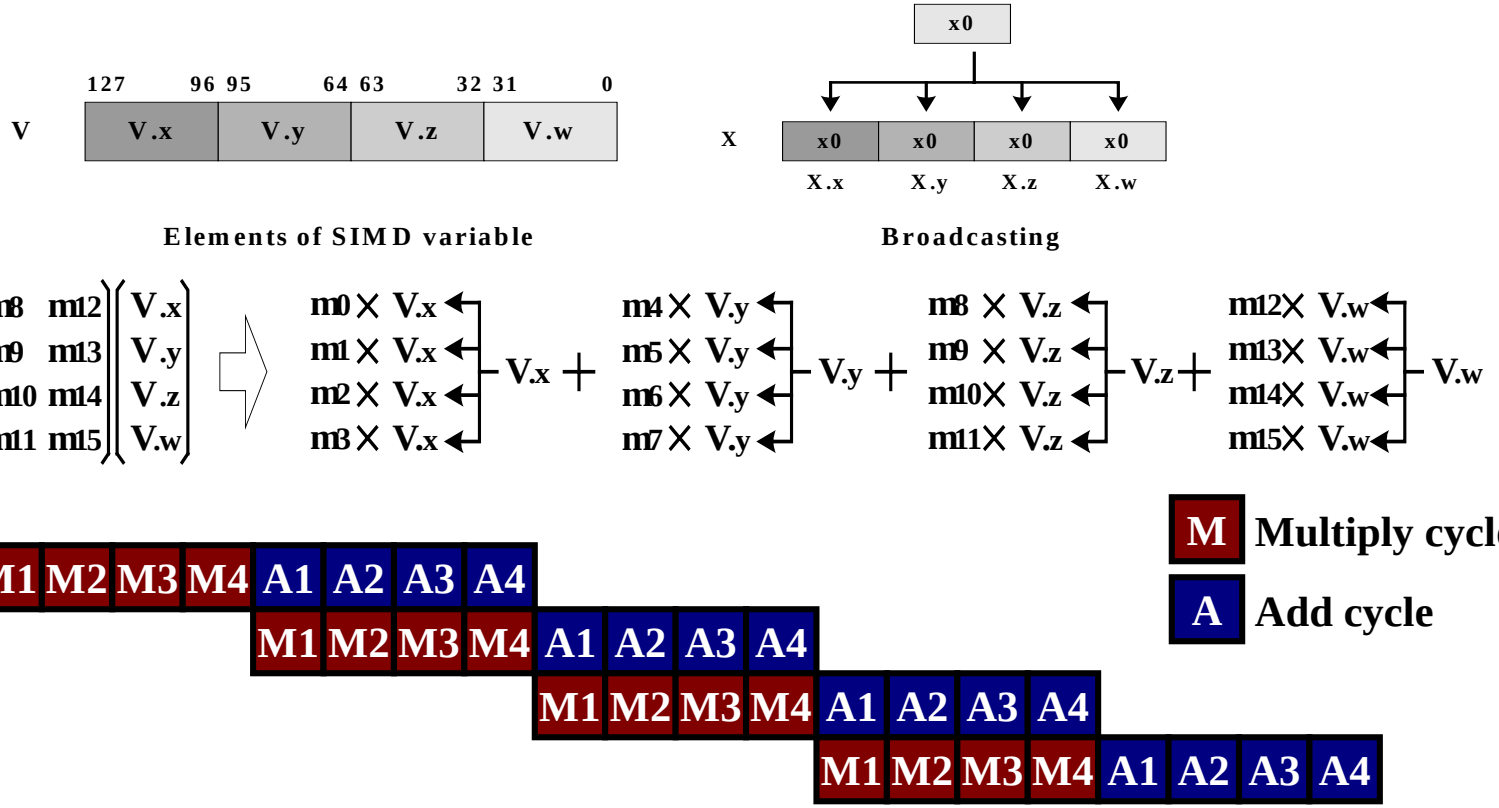
SATINE

- **Architecture**
  - **SIMD coprocessor**
    - **Brings new 53 instructions**
    - **4 Way 128 bit integer SIMD datapath**
    - **Datapath**



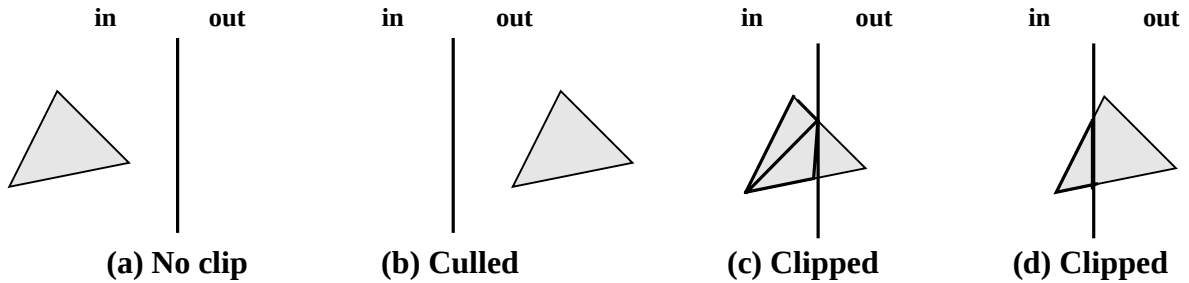
SATINE

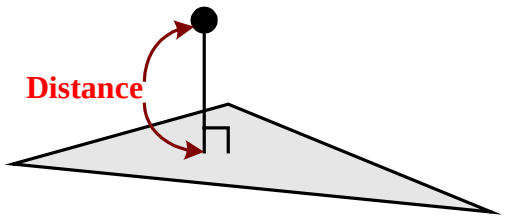
- **Architecture**
  - **SIMD acceleration for 3D operations (1)**
    - **Vertex transformation: VMMV instruction**



SATINE

- **Architecture**
  - **SIMD acceleration for 3D operations (2)**
    - **Clip operations : TCLIP instruction**

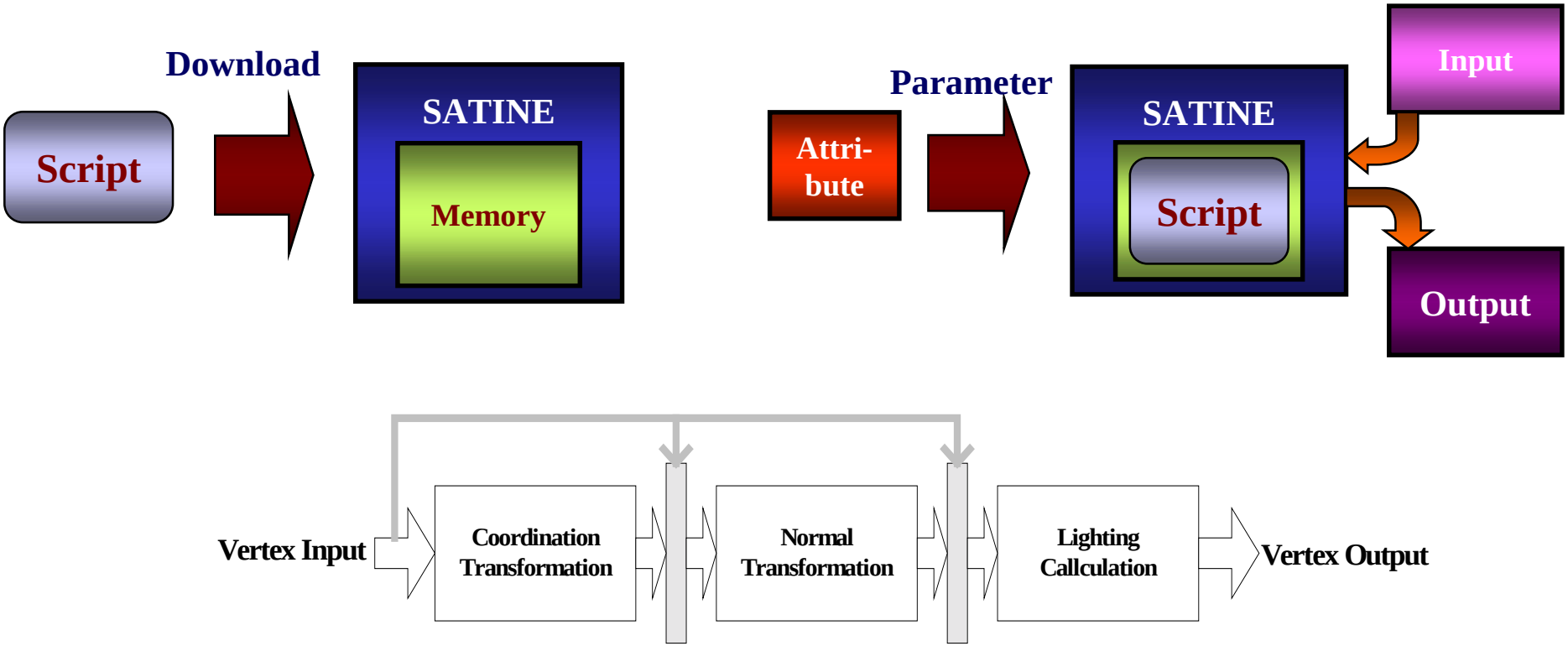




$$dist = v.x \times plane.x + v.y \times plane.y + v.z \times plane.z - v.w \times plane.w$$

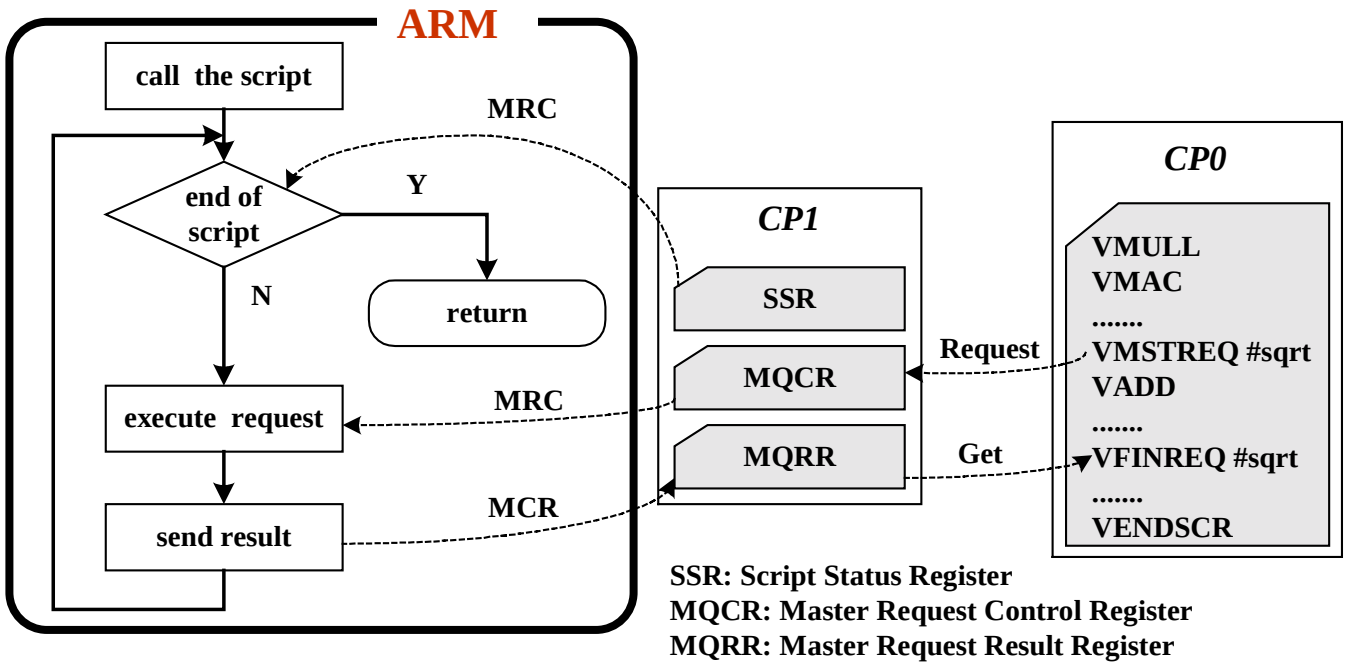
SATINE

- **Architecture**
  - **Script Execution and Stream Processor**



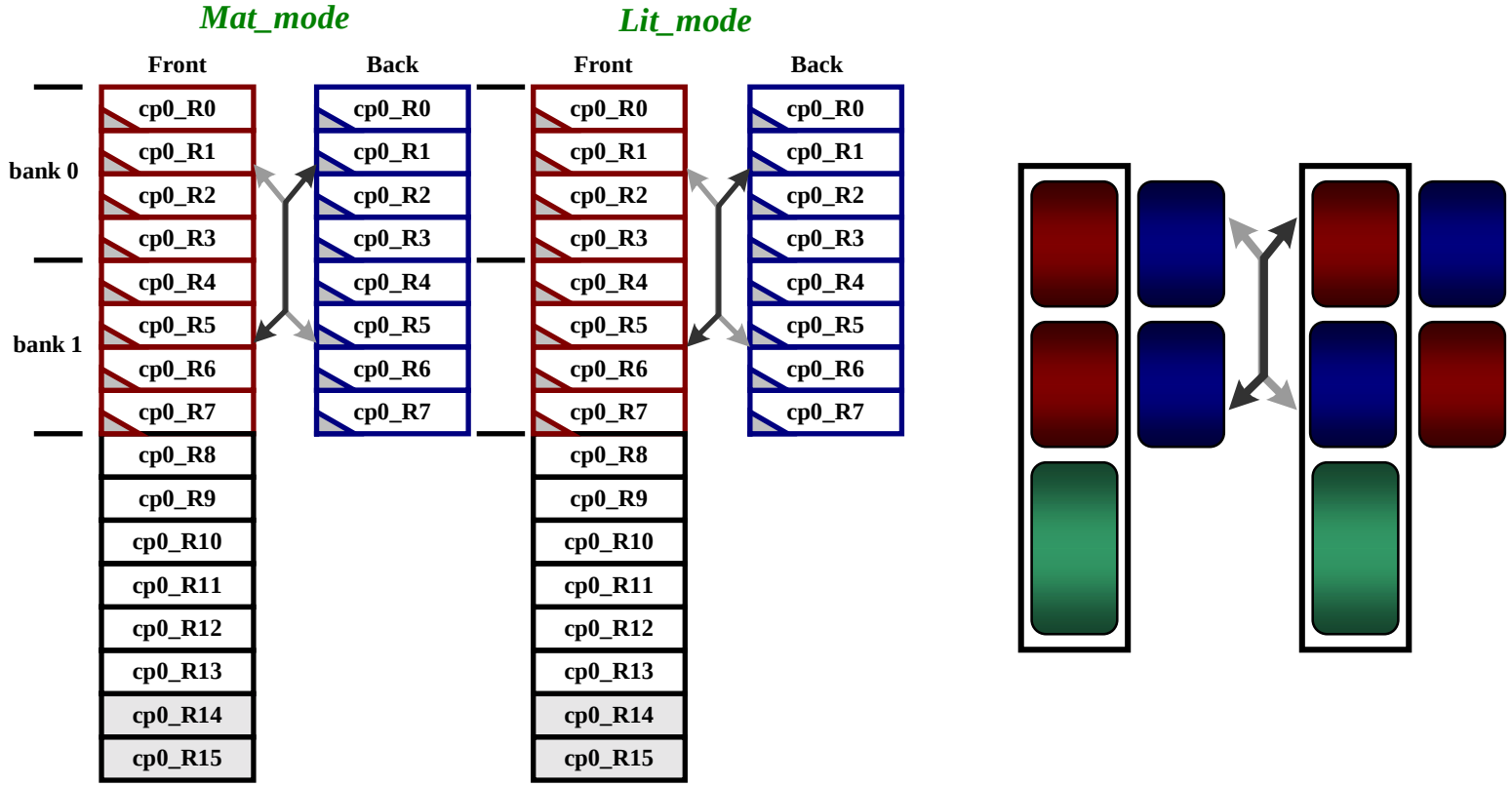
SATINE

- **Architecture**
  - **Master Request Interface (MRI)**
    - **C/Assembly function in ARM and SATINE script can be executed with passing the parameters in parallel**
    - **DIV/SQRT**



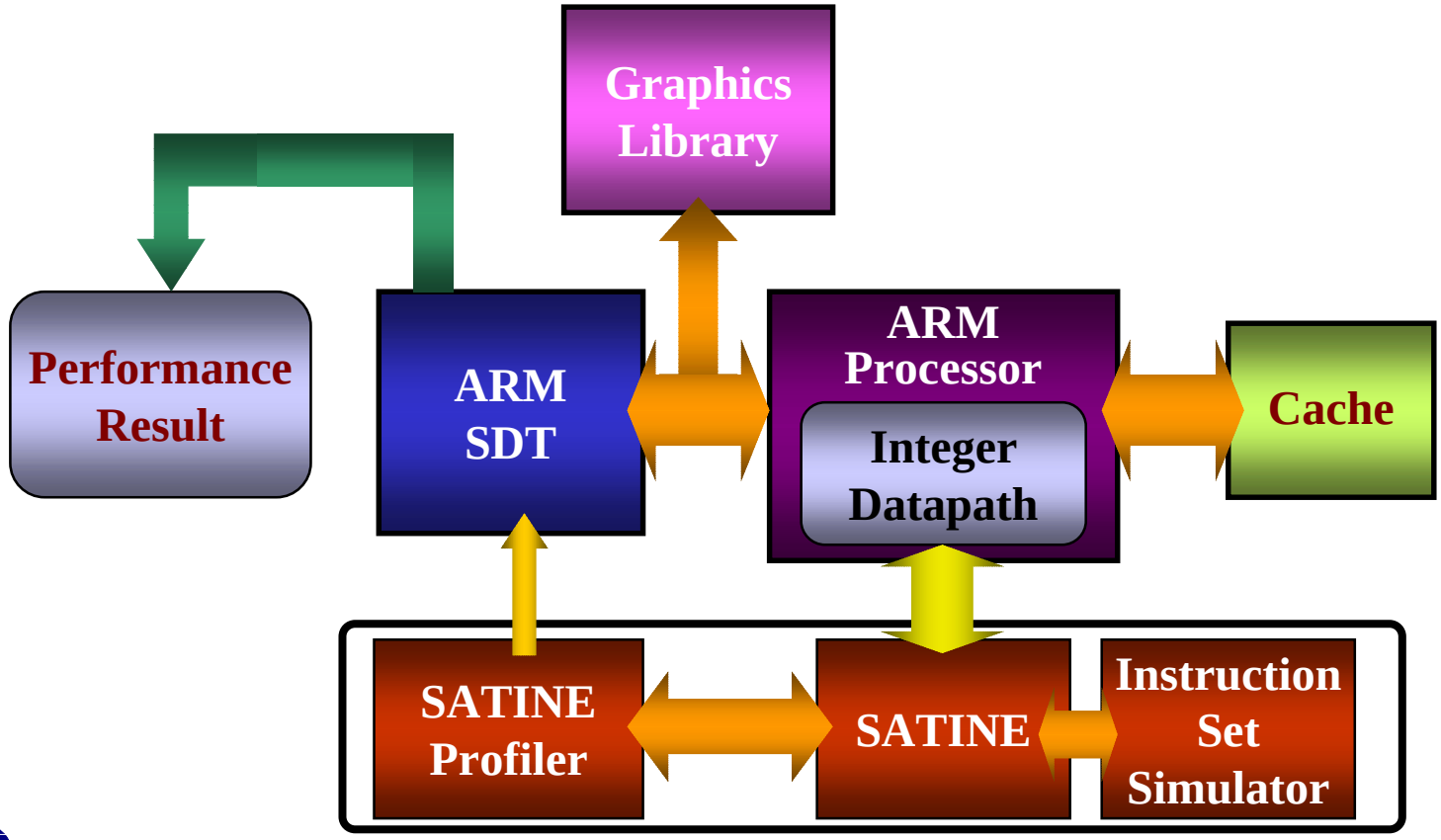
SATINE

- **Architecture**
  - **Multi-Mode Register File**
    - **For efficient register use in 3D operations**



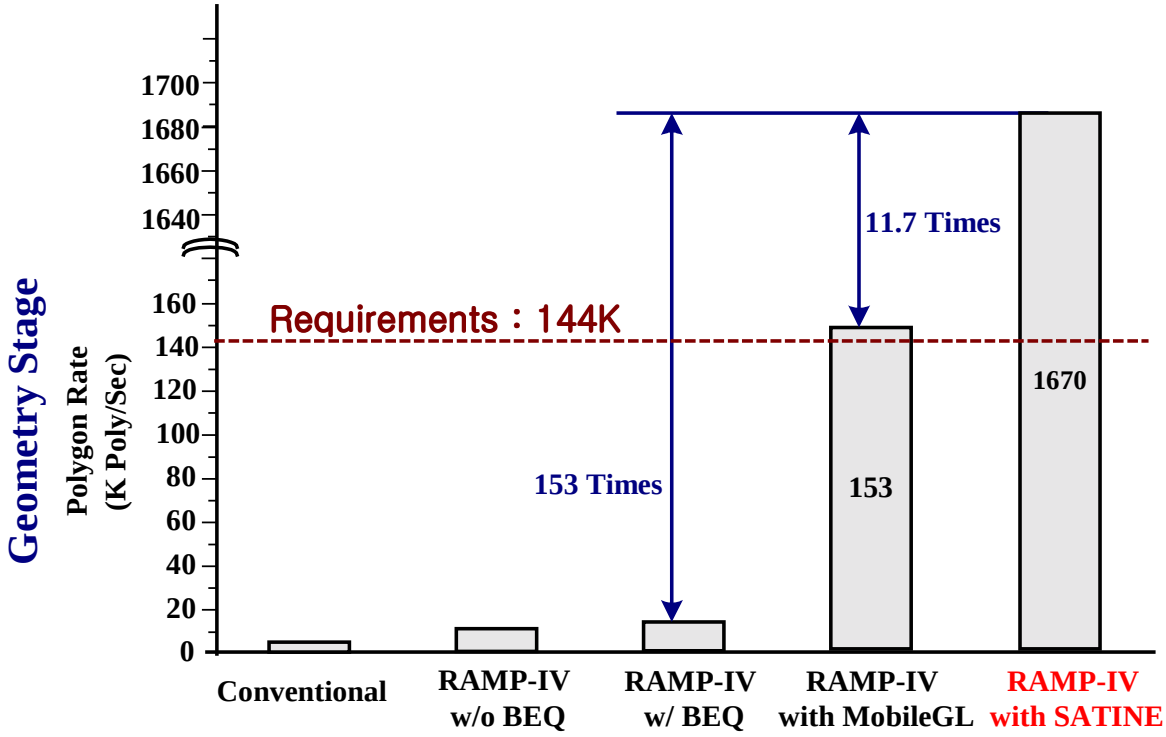
SATINE

- **Performance Estimation**
  - **Simulation Environment**



SATINE

- **Performance Estimation**
  - **Estimated performance**
    - **SATINE @200㎒ with ARM9**



SATINE

- **Performance Estimation**
  - **Estimated Layout Area**
    - **1.48 times of ARM9**

		Gate counts	Layout area (0.16 ㎛ DRAM)
ARM9		47095	2.17 ㎜ by 2.17㎜
SATINE	Others	39622	2.7 ㎜ by 2.7㎜
	Multipliers	21868	
	ALUs	8024	

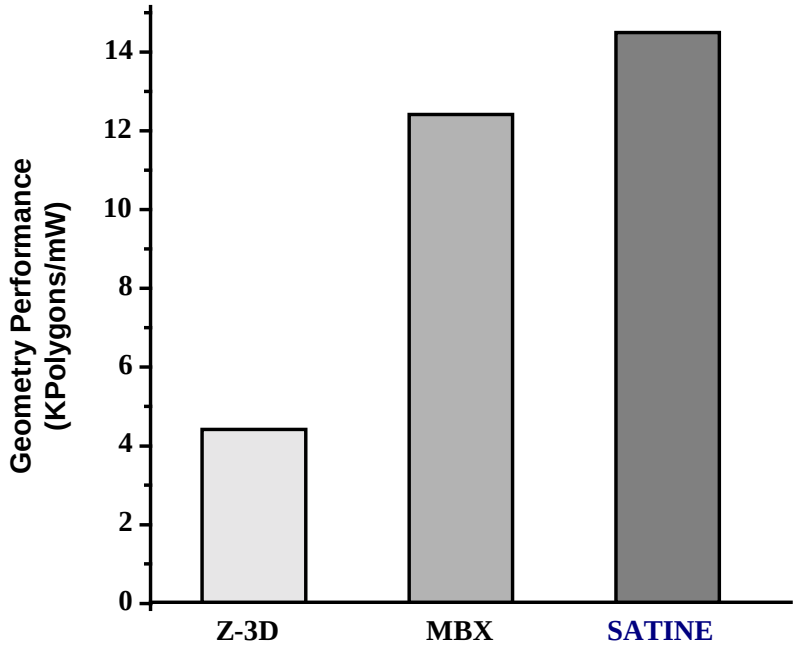
  - **Estimated Power Consumption**

		Power	Speed
ARM9		42㎽	200㎒. (assumption)
SATINE	Un-lit polygon	36.7㎽	200㎒.
	Lit polygon	52.8㎽	200㎒.

SATINE

- **Performance Estimation**
  - **Performance Comparison**

$$3D\,Geometry\,Performance = \frac{Polygon\,Calculation\,Rate}{Power\,Consumption}\ (KPolygons/mW)$$



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- **Conclusion and Further Works**

Conclusion and Further Works

- **Conclusion**
  - **Efficient interface block for portable 3D processor was implemented**
    - **0.16 um DRAM process**
    - **3.5 mW power consumption with reduced communication cost**
  - **Mobile graphics library was developed by system level simulation for RAMP-IV portable multimedia processor**
    - **153K polygon/sec with fixed point arithmetic**
  - **3D Geometry coprocessor suitable for mobile applications was proposed**
    - **1.67M polygon/sec**

- **Further work**
  - **Hardware implementation of proposed architecture**